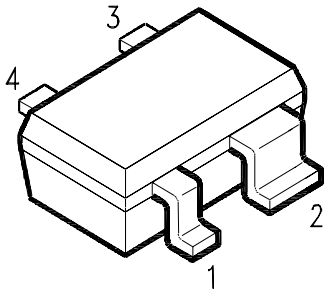
A Low-Cost, Two-Stage Low Noise Amplifier for 5 – 6 GHz Applications Using the Silicon-Germanium BFP640 Transistor

- **High Gain (20 dB minimum over 5 – 6 GHz range)**
- **Excellent Noise Figure: 1.4 dB @ 5470 MHz for two-stage cascade**
- **Good Linearity: Input 3rd Order Intercept = + 5 dBm**
- **High Reverse Isolation (> 30 dB)**
- **Outstanding price / performance ratio**
- **Low Power Consumption: 16 mA @ 3.3V**
- **Low PCB Area required (≅ 80 mm^2 for complete LNA)**
- **Applications: 5 – 6 GHz WLAN systems, 5 GHz Cordless Phones, other 5 GHz Systems**



1	2	3	4
B	E	C	E

1. Introduction

Infineon Technologies' **BFP640 Silicon Germanium RF Transistor** is shown in a two-stage Low Noise Amplifier ("LNA") application targeted for Wireless LAN and other systems using the frequency range from 5 to 6 GHz. The **BFP640** offers a remarkably low noise figure, high gain and excellent linearity at an unbeatable price-to- performance ratio, enabling the circuit designer to utilize low-cost, highly repeatable bipolar technology in industry-standard surface-mount packaging at frequencies previously attainable only with the use of more expensive device processes such as Gallium Arsenide. **Figure 2** on page 3 shows Infineon Technologies current SiGe transistor family, and **Figures 6 and 7** on page 7 give a schematic diagram and Bill Of Material (BOM) for the LNA.

Measurement results are presented in **Table 1.** These results are mean values taken from a sample lot of 12 circuit boards. Please note that the reference planes for all measurement data shown in **Table 1** are at the PC board's SMA RF connectors; in other words, if losses at the LNA input were subtracted, the noise figure values would be slightly lower than shown. **Section 2** of this Applications Note gives an overview of the **BFP640** and Infineon's SiGe RF Transistor products and **Section 3** provides LNA design details including 1) a schematic diagram 2) a Bill Of Material (BOM) 3) photos of the PCB 4) a PCB cross-section diagram. **Appendix A** on page 10 has complete electrical data including minimum, maximum, mean value, and standard deviation for a sample lot of 12 Printed Circuit Boards (PCBs). Data plots from a sample board are given in **Appendix B** beginning on page 11, and temperature test data for the -40 to +85 °C range is located in **Appendix C** beginning on page 21.

Table 1. Typical performance, complete Two-Stage 5 – 6 GHz BFP640 LNA, T=25°C.

Conditions: Temperature=25°C, V=3.3 Volts, n=12 units, Z_S=Z_L=50Ω, network analyzer source power = -30 dBm

Parameter	Frequency, MHz		
	5150	5470	5925
Gain, dB	23.5	22.2	20.3
Noise Figure, dB	1.3	1.4	1.5
Input IP_3, dBm	---	+ 5.0	---
Input P_{1dB}, dBm	---	-14.2	---
Input Return Loss, dB	15.3	19.0	16.4
Output Return Loss, dB	10.9	14.7	17.0
Supply Current, mA	16.3		
PCB Area, mm^2	80 mm^2		
Number of SMT components*	25		

* Includes bias resistors, DC blocks, chip coils & BFP640's

2. Description of the BFP640 and Infineon's SiGe Transistor Family

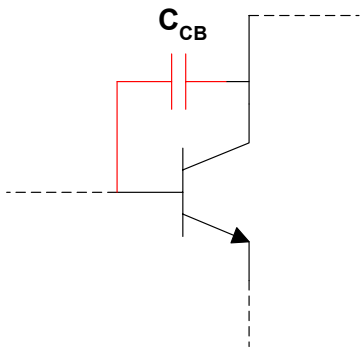
The **BFP640** is a Silicon-Germanium (SiGe) heterojunction bipolar transistor manufactured in Infineon Technologies' B7HF process. The BFP640 is a derivative of Infineon's original SiGe transistor, the **BFP620**. While sharing the same basic transistor die, the BFP640 has been enhanced to provide improved performance characteristics as compared to the BFP620, while maintaining the BFP620's phenomenally low noise figure levels. These improvements bring the world-class, cost-effective performance of the BFP620 to an even higher level.

In the BFP640, a lower or "lighter" dopant concentration in the transistor's collector region is used. The lighter collector doping increases the minimum collector-emitter breakdown voltage (V_{CEO}), reduces the transistor's internal parasitic collector-base capacitance ($C_{CB,}$ **Figure 1**) and reduces undesired internal feedback, yielding increased gain and improved stability margin.

Figure 1. Process enhancements for BFP640, BFP650 and BFP690 transistors increase the minimum collector-emitter breakdown voltage (from 2.3 to 4.0V V_{CEO}) and reduce the transistor's internal parasitic capacitance $C_{CB.}$ This results in a reduction in reverse transmission coefficient S12, yielding higher gain & improved stability.

C_{CB} reduced via lighter collector doping

=> Higher Breakdown Voltage
=> Higher Gain
=> Improved Stability Margin



The higher minimum breakdown voltage of the BFP640 (4.0 Volts V_{CEO}, versus 2.3 V for the BFP620) makes operation in 3 volt systems more convenient, as it is not possible to exceed the BFP640's maximum collector-emitter voltage in a system using a 3 volt power supply. The higher breakdown voltage permits the elimination of circuit elements previously needed to reduce the 3V system supply voltage to below 2.3 volts, which were required for safe operation with the older BFP620. In addition to being useful in LNA applications, the BFP640 has been successfully employed as a Power Amplifier Driver (PA Driver) in 5 GHz WLAN designs.

The BFP640's two siblings, the **BFP650** and **BFP690**, utilize the same process enhancements as the **BFP640**, but have larger emitter areas, allowing for increased collector current and higher RF output power levels. The maximum ratings for the BFP640, BFP650 and BFP690 are given in **Table 2** below. A chart showing details of Infineon Techologies' current SiGe transistor offering is given on the next page, in **Figure 2**.

Table 2. Overview of Maximum Ratings and Packaging for Infineon Technologies SiGe RF Transistors BFP620, BFP640, BFP650 and BFP690.

Device	V_{CEO} Volts	$I_{C\ MAX}$, mA	P_{DISS}, mW	R_{thJS}*	Package
BFP620	2.3	80	185 (1)	≤ 300 °C /W	SOT343
BFP620F	2.3	80	185 (1)	≤ 280 °C /W	TSFP4
BFP640	4.0	50	200 (2)	≤ 300 °C /W	SOT343
BFP650	4.0	150	500 (3)	≤ 140 °C /W	SOT343
BFP690	4.0	350	1000 (4)	≤ 60 °C /W	SCT595

* Thermal resistance, device junction to soldering point

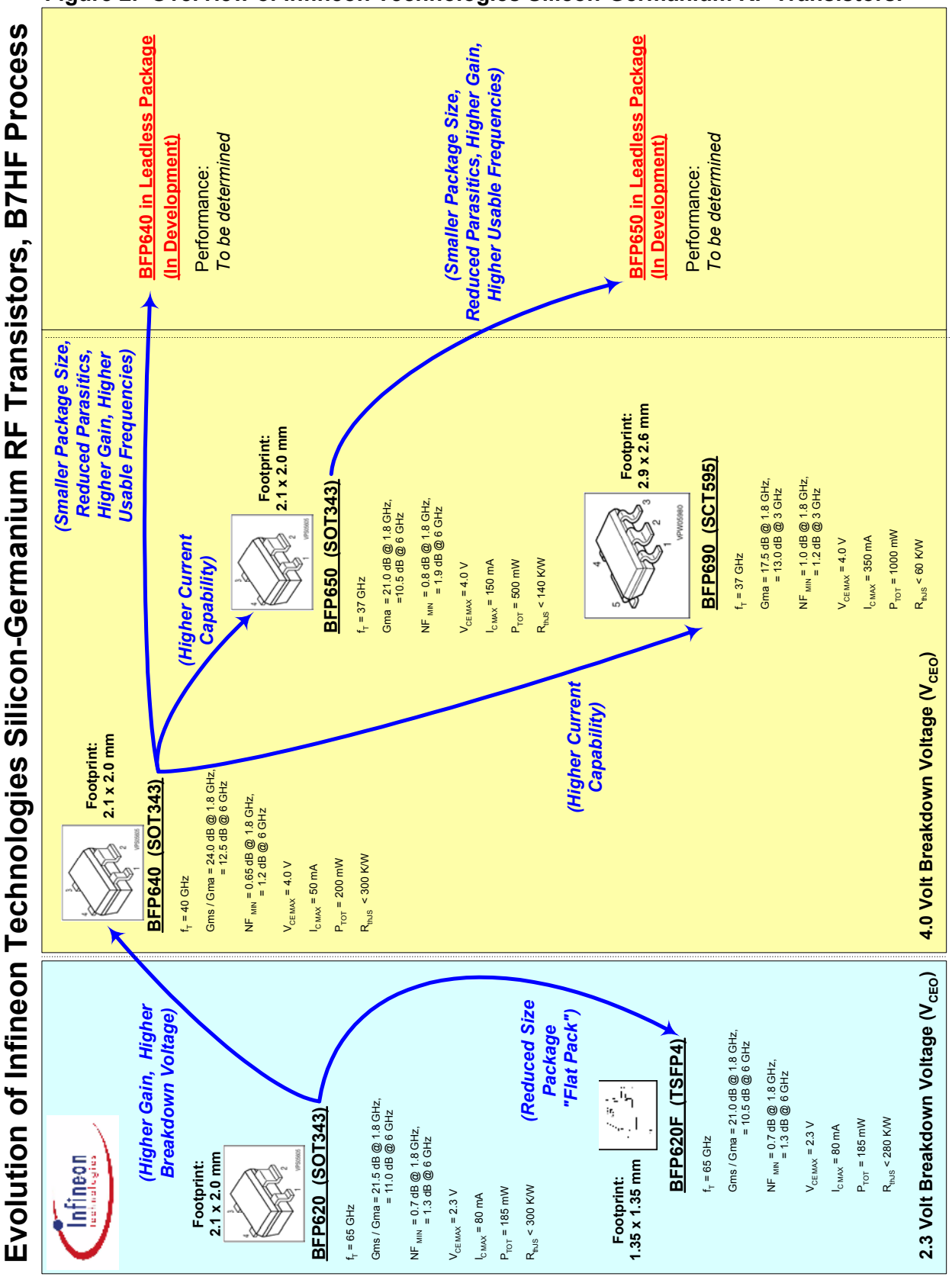
(1) Soldering point temperature ≤ 95 °C

(2) Soldering point temperature ≤ 90 °C

(3) Soldering point temperature ≤ 75 °C

(4) Soldering point temperature ≤ 80 °C

Figure 2. Overview of Infineon Technologies Silicon-Germanium RF Transistors.



3. 5 - 6 GHz Two-Stage LNA Design Details

Overview

The LNA consists of two identical BFP640 stages in cascade. All RF simulations and Printed Circuit Board design steps took place within the **Eagleware GENESYS®** [1] software design package. Effort was made to minimize noise figure as well as the number of external matching elements required. The circuit board is laid out in such a manner as to permit easy testing of either stage individually. Lumped element matching techniques are used exclusively to minimize required PC Board area.

Stability

In general, for a linear two-port device characterized by s-parameters, the two necessary and sufficient conditions to guarantee unconditional stability (e.g. no possibility of oscillation when the input and output of the device are both terminated in any passive real impedance) are

a) $\mathbf{K} > \mathbf{1}$ and b) $|\Delta| < \mathbf{1}$ where

$$\mathbf{K} = \frac{\mathbf{1} - |\mathbf{s11}|^2 - |\mathbf{s22}|^2 + |\Delta|^2}{\mathbf{2}|\mathbf{s12} \cdot \mathbf{s21}|}$$

$$|\Delta| = |\mathbf{s11} \cdot \mathbf{s22} - \mathbf{s12} \cdot \mathbf{s21}|$$

In the literature one may encounter an alternative form for these two conditions as

a) $\mathbf{K} > \mathbf{1}$ and b) $\mathbf{B_1} > \mathbf{0}$ where

$$\mathbf{B_1} = \mathbf{1} + |\mathbf{s11}|^2 - |\mathbf{s22}|^2 - |\Delta|^2$$

A single stage of the two-stage LNA was measured for S-parameters from 125 MHz to 2 GHz, & then from 2 – 15 GHz. The S-parameter files from each measurement were imported into the **Eagleware GENESYS®** package. GENESYS was employed to calculate and plot Stability Factor "K" & Stability Measure "B_1" in each case. Refer to **Figures 3 and 4** on the next page. One can see K>1 and B_1>0, showing that the necessary and sufficient conditions for unconditional stability have been met. Since both stages are of identical design and layout, it is sufficient to check for unconditional stability of either one of the two stages. If the criteria for unconditional stability are satisfied for a single stage, than an additional identical stage may be safely cascaded after the first stage, provided the two stages don't have an undesired feedback path between them. In other words, unless the individual unconditionally stable stages can "talk" to each other via leakage paths through shared DC supply lines or other PC board features, cascading individual unconditionally stable stages will result in an unconditionally stable multi-stage amplifier.

In making stability calculations using measured S parameters, one must bear in mind that the reverse transmission coefficient (S12) of high-transition frequency devices like the BFP640 becomes vanishingly small at lower frequencies. Therefore, the signal being measured may well fall into the noise floor of the network analyzer being used. It's important that network analyzer dynamic range considerations are taken into account when making the S-parameter measurements. Otherwise, the measured S-parameter results may be suspect, and one may not get a "clean curve" when plotting K and B_1 – particularly for frequencies below 1 GHz. An excellent reference for the interested reader is given in [2].

Linearity

This LNA makes use of a "trick" to enhance third-order intercept performance. In brief, a relatively large-value capacitor is placed across the base-emitter and collector-emitter junctions to provide a low impedance path at low frequencies. This low-frequency path serves to bypass the low-frequency difference product (f_2-f_1) resulting from a two-tone test. (See schematic on page 7; C3, C8, C6 and C11 perform this function). A rule of thumb states that there exists approximately 10 dB difference between the amplifier compression point and the third order intercept point. Use of this "trick" gets around this general rule, and increases the difference from the expected 10 dB to between 15 and 20 dB. Employment of this technique is why the LNA's input third order intercept point (**IIP_3**) of +5.0 dBm is more than 10 dB higher than the amplifier's typical input 1dB compression point (IP_{1dB}) of –14 dBm. For additional detail on how this "capacitor trick" works, please refer to reference [3].

Figure 3. Stability Factor "K" and Stability Measure "B1" for one stage of the 5 GHz LNA. The frequency range for this plot is 125 MHz to 2 GHz. Note that K>1 and B_1 >0. The plot is generated in Eagleware's GENESYS® simulator, from a measured amplifier S-parameter file.

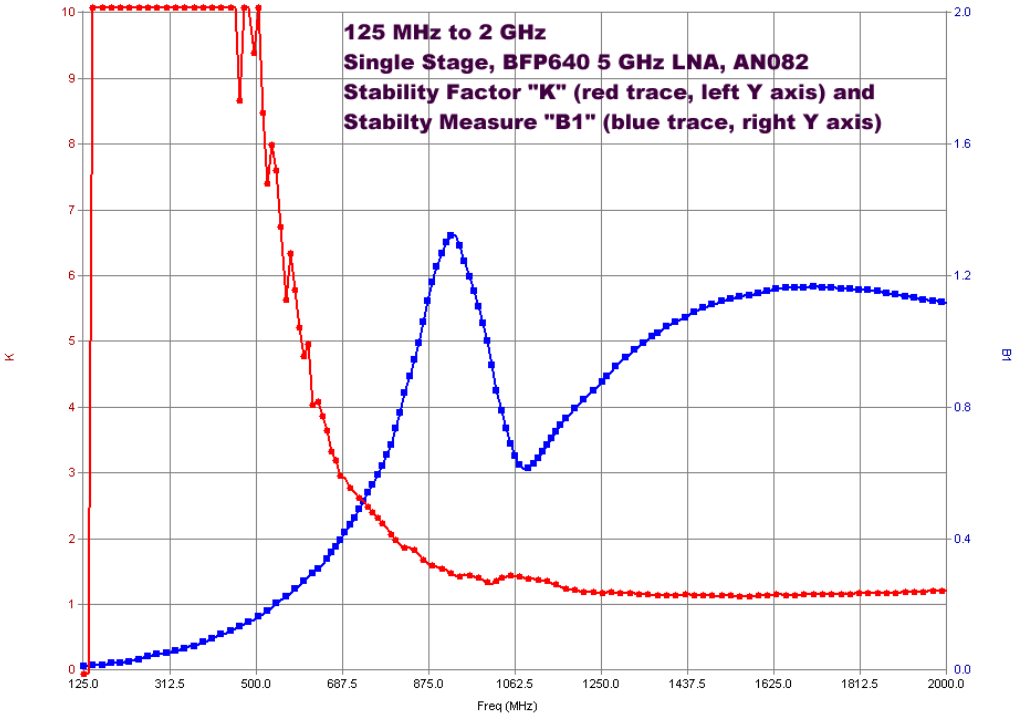
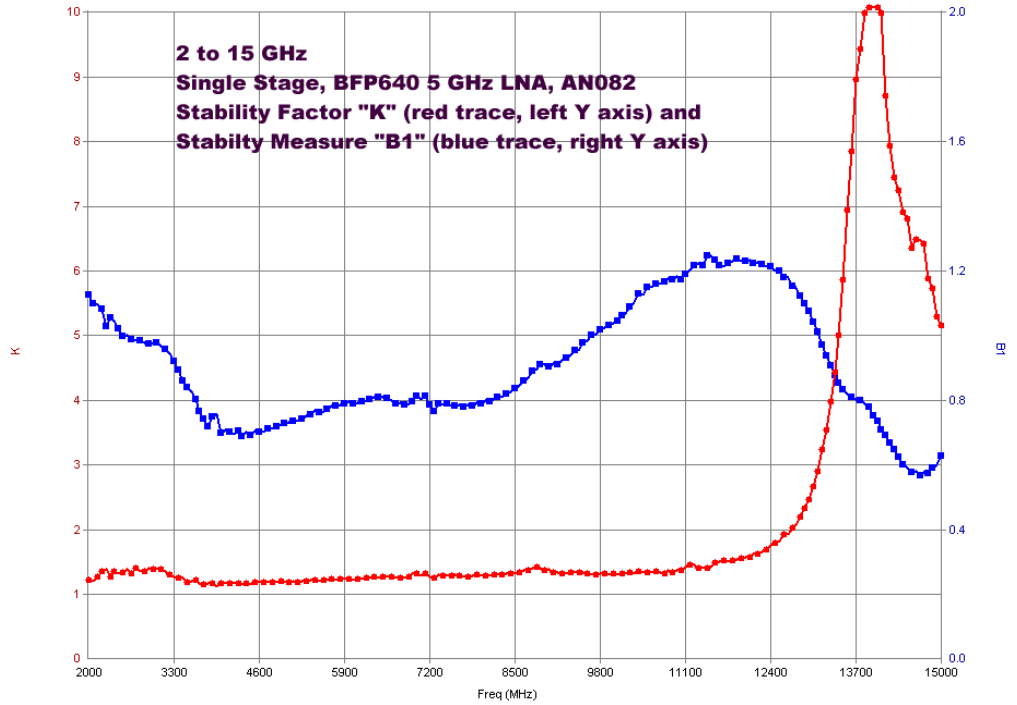


Figure 4. Stability Factor "K" and Stability Measure "B1" for one stage of the 5 GHz LNA. The frequency range for this plot is 2 GHz to 15 GHz. Note that K>1 and B_1 >0. The plot is generated in Eagleware's GENESYS® simulator, from a measured amplifier S-parameter file.



Noise Figure

The BFP640 is an excellent low-noise device and offers noise figure performance comparable to far more expensive GaAs MESFET and GaAs PHEMT devices. Unlike GaAs FETs, no negative supply voltage is required with bipolar heterojunction transistors like the BFP640.

As one would expect with RF transistors housed in standard, low-cost surface-mount packaging, the gain of the BFP640 transistor chip is limited by the package parasitics as one moves above the 3 GHz range. Near 5 GHz, the bias current for minimum noise figure is about 5 mA. A tradeoff of gain, noise figure and linearity resulted in the DC operating point of 3 volts V_{CE} and 8 mA collector current being selected. **Table 3** below gives noise parameters for the BFP640 at the 3 volt, 8 mA bias point. Note the excellent minimum noise figure values (F_{MIN}) and the modest, easy-to-handle optimum reflection coefficient magnitudes (Γ_{OPT}). The superb minimum noise figure values, coupled with the relatively low reflection coefficient magnitudes required for achieving minimum noise figure amplifier designs makes the BFP640 easy to work with. The BFP640 enables the circuit designer to create LNAs which are forgiving of variations in PC board characteristics and tolerances in chip components.

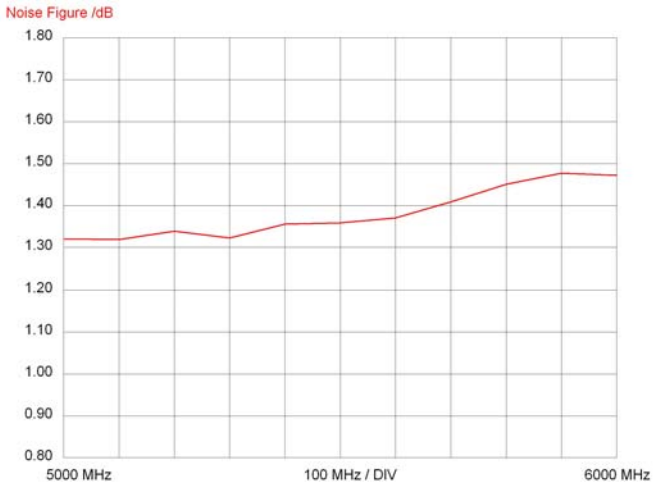
Table 3. BFP640 device Noise Parameters at V_{CE} = 3.0V, I_C = 8 mA.

Freq. (GHz)	F_{MIN} (dB)	Γ_{OPT} (mag)	Γ_{OPT} (angle)	$R_N/50$ (ohms)
0.9	0.42	0.22	21	0.12
1.8	0.68	0.08	2	0.11
2.4	0.74	0.08	50	0.11
3.0	0.84	0.06	141	0.09
4.0	0.91	0.11	-101	0.10
5.0	1.01	0.25	-61	0.14
6.0	1.20	0.22	-82	0.13

In designing the LNA for both low parts count and best possible noise figure, it was decided to avoid any external input impedance matching elements, if at all possible. In addition to the possibility of pulling the input impedance presented to the transistor further away from it's optimum impedance for noise figure, any practical matching element will introduce loss of some sort at the LNA input and therefore degrade the amplifier noise figure. This is especially true up at 5 GHz. The next section describes how a compromise between good return loss and minimum noise figure was achieved.

A plot of noise figure vs. frequency for the two-stage cascade LNA is given in **Figure 5.**

Figure 5. Noise Figure at T = 25°C for the complete two-stage cascaded BFP640 LNA.



Input / Output Impedance Match

Please refer to the schematic diagram in **Figure 6** on the following page. Lumped-element matching techniques are used exclusively, to reduce required PC board area. The output impedance matching circuit consists of L2 and L3 for the first stage, and L5 + L6 for the second stage. Due to the nonzero reverse transmission coefficient of the transistor (S12 $\neq$ 0), the output match favorably influences the input impedance match, with better than 10 dB input and output return loss values achieved across the band. As a result, no input impedance matching elements are required – only an input DC block and a "choke" (L1 on first stage) to bring in base bias current is needed at the input. The value of L1 and L4 were chosen such that the chip coils operate just below their self-resonant frequency (SRF), ensuring that these elements have minimal loading effects on the input of each stage. A Bill Of Material (BOM) is presented in **Figure 7** (below the schematic diagram). Note that low-cost, industry-standard 0402 case-size chip components are used throughout.

Figure 6. Schematic Diagram for the Complete Two-Stage 5 – 6 GHz LNA.

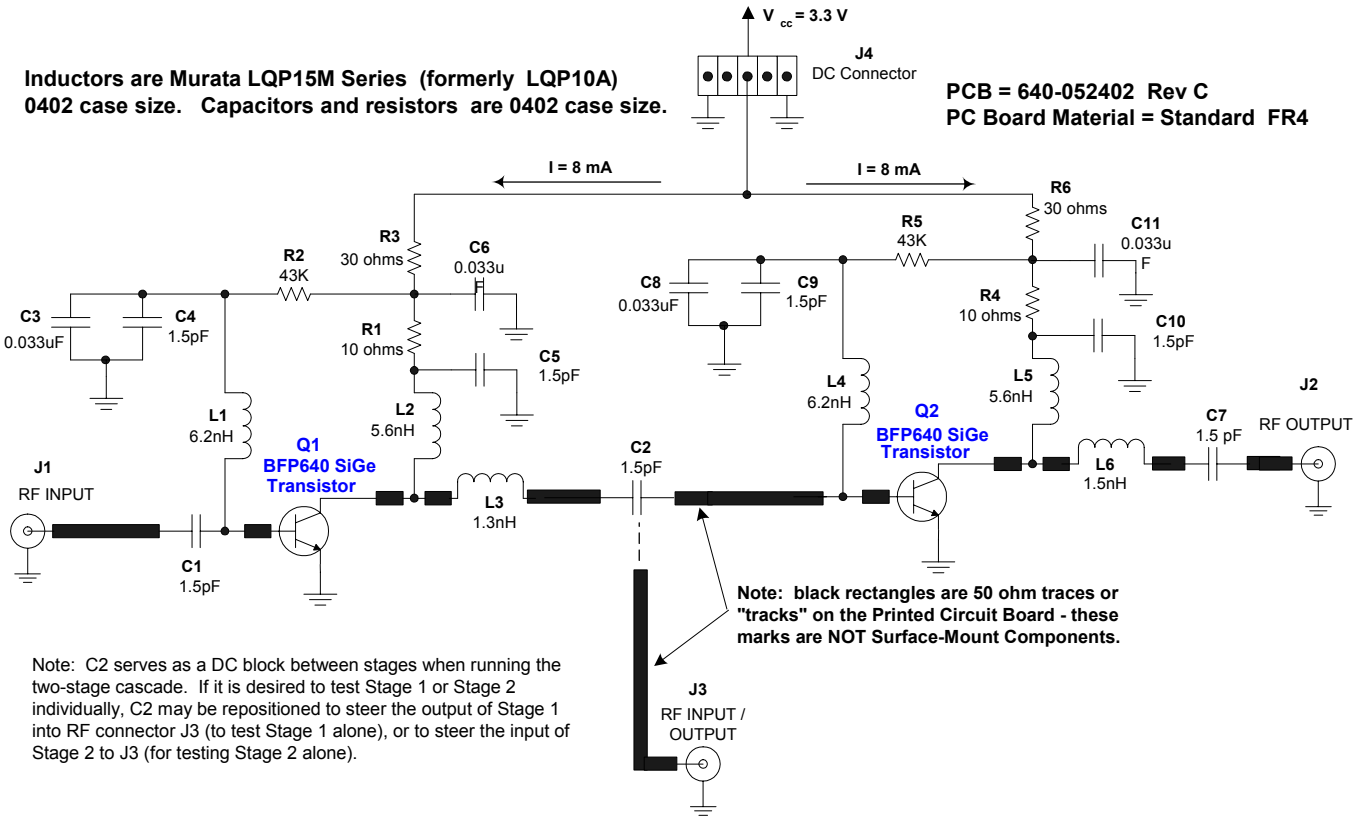


Figure 7. Bill Of Material (BOM) for the complete two-stage LNA.

REFERENCE DESIGNATOR	VALUE	MANUFACTURER	CASE SIZE	FUNCTION
C1, C2, C7	1.5 pF	VARIOUS	0402	DC BLOCKING
C4, C5, C9, C10	1.5 pF	VARIOUS	0402	RF BYPASS / RF BLOCK
C3, C6, C8, C11	0.033 μF	VARIOUS	0402	LOW FREQUENCY GROUND AT BASE (INPUT 3RD ORDER INTERCEPT IMPROVEMENT), LOW-FREQUENCY DECOUPLING / BLOCKING
L1, L4	6.2 nH	MURATA LQP15M SERIES TIGHT TOLERANCE INDUCTOR (FORMER MURATA SERIES = LQP10A)	0402	RF "CHOKE" TO DC BIAS ON BASE OF Q1 AND Q2
L2, L5	5.6 nH	MURATA LQP15M TIGHT TOLERANCE INDUCTOR	0402	RF 'CHOKE' TO COLLECTOR OF Q1 AND Q2; ALSO INFLUENCES OUTPUT MATCH OF EACH STAGE
L3	1.3 nH	MURATA LQP15M TIGHT TOLERANCE INDUCTOR	0402	OUTPUT MATCHING, STAGE 1
L6	1.5 nH	MURATA LQP15M TIGHT TOLERANCE INDUCTOR	0402	OUTPUT MATCHING, STAGE 2
R1, R4	10 ohms	VARIOUS	0402	FOR STABILITY, OUTPUT MATCHING
R2, R5	43K	VARIOUS	0402	DC BIAS FOR BASE OF Q1, Q2
R3, R6	30 ohms	VARIOUS	0402	DROP SUPPLY VOLTAGE BY APPROX. 0.3V, PROVIDE DC FEEDBACK FOR BIAS COMPENSATION (BETA VARIATION, TEMP., ETC.)
Q1, Q2	**-**	**INFINEON TECHNOLOGIES**	**SOT-343**	**BFP640 SiGe Transistor, 40 GHz f_T**
J1, J2, J3	-	JOHNSON 142-0701-841	-	RF INPUT / OUTPUT CONNECTORS (J2 ONLY USED WHEN TESTING STAGES INDIVIDUALLY)
J4	-	AMP 5 PIN HEADER MTA-100 SERIES 640456-5 (STANDARD PIN PLATING) **OR** 641215-5 (GOLD PLATED PINS)	-	DC CONNECTOR PINS 1, 5 = GROUND PIN 3 = V_{CC} PINS 2,4 = NO CONNECTION

Details on the Printed Circuit Board

As stated previously, the PC board used in this applications note was simulated within and generated from the **Eagleware GENESYS®** software package. After simulations, CAD files required for PCB fabrication, including Gerber 274X and Drill files, were created within and output from GENESYS. Photos of the PC board are provided in **Figures 8, 9 and 10**. A cross-sectional diagram of the PCB is in **Figure 11**.

The PC Board material used is standard low-cost FR4. Note that each stage of the LNA may be tested individually; capacitor C2 (see schematic) may be positioned to "steer" the RF from the output of the first stage to the SMA connector on the bottom of the PCB, or, C2 may be used to link the track from this same RF connector to the input of the second stage, to permit testing of Stage 2 individually. The total PCB area consumed for a single stage is approximately 0.300 x 0.200 inch / 7.6 x 5.1 mm, or approximately 40 mm^2, giving about 80 mm^2 for the complete two-stage amplifier. The total component count, including all passives and the two BFP640 transistors, is 25.

Figure 8. Top View of 5 GHz LNA PC Board.

Figure 9. Bottom View of LNA PC Board.

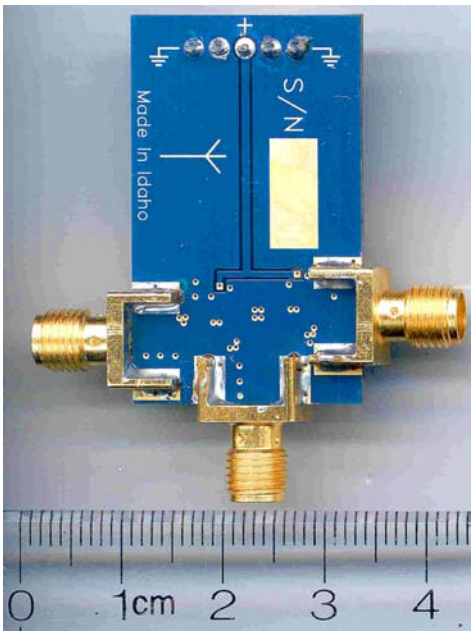


Figure 10. Close-In Shot of PCB showing component placement.

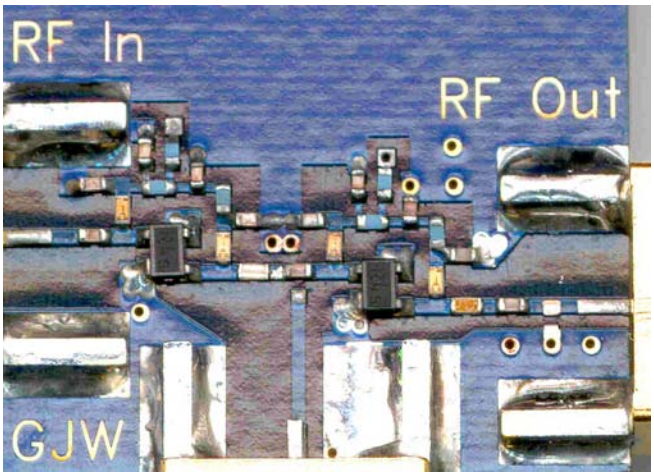
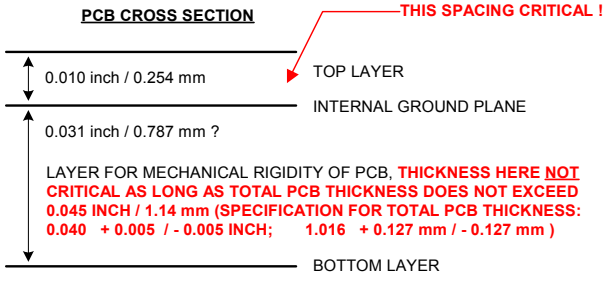


Figure 11. Cross-Section Diagram of the LNA Printed Circuit Board. Note spacing between top layer RF traces and internal ground plane is 0.010 inch / 0.254 mm.



4. Conclusions

Infineon Technologies' BFP640 Silicon-Germanium RF transistor offers a very high performance, power-efficient and cost-effective solution for a broad range of high-frequency low-noise amplifier (LNA) designs. The BFP640 improves on the world-class performance of its predecessor, the BFP620. There are other SiGe transistors in Infineon's high-frequency transistor family, covering a full spectrum of applications and output power requirements. The flexibility of these devices allows one part to fulfill several different functions. For example, the BFP640 may be used as an LNA or a PA Driver amplifier in 5 GHz WLAN applications.

This applications note describes a high-performance, low cost, lumped-element discrete LNA design for the 5 – 6 GHz frequency range. Evaluation boards for the LNA application shown in this applications note are available from Infineon Technologies. The company's website is http://www.infineon.com and further information on Infineon's Silicon Discretes products may be found at http://www.infineon.com/cgi/ecrm.dll/ecrm/scripts/prod_cat.jsp?oid=-8145 .

References

[1] Eagleware Corporation, 653 Pinnacle Court, Norcross, GA 30071 USA. Tel: +1.678.291.0995 http://www.eagleware.com

Eagleware software suite GENESYS Version 8 was used in all simulation, synthesis, and PC board CAD file generation done for the circuit described in this Applications Note.

[2] "Understanding and Improving Network Analyzer Dynamic Range", application Note 1363-1, Agilent Technologies.

This applications note explains how to minimize the noise floor / maximize the dynamic range of your network analyzer.

[3] "A High IIP_3 Low Noise Amplifier for 1900 MHz Applications Using the SiGe BFP620 Transistor". Applications Note AN060, Silicon Discretes Group, Infineon Technologies.

The section entitled "Effect of adding additional charge-storage across the base-emitter junction" explains the "capacitor trick" used to enhance third-order intercept performance.

Appendixes on following pages =➔

Appendix A. Data on 12 two-stage BFP640 LNA Circuit Boards, 640-052402 Rev C, taken randomly from a batch of assembled units. All data taken at room temperature (25°C).

Board S/N	dB[s11]^2			dB[s21]^2			dB[s22]^2			Noise Figure, dB			Input IP_3, dBm	Input P_{1dB}, dBm	Current Consumption mA
	5150 MHz	5470 MHz	5925 MHz	5150 MHz	5470 MHz	5925 MHz	5150 MHz	5470 MHz	5925 MHz	5150 MHz	5470 MHz	5925 MHz	5470 MHz	5470 MHz	
002	15.2	17.7	15.1	23.4	22.1	20.2	10.2	13.0	16.3	1.3	1.4	1.5	+6.9	-14.3	16.4
005	16.9	21.1	15.9	24.0	22.7	20.6	11.9	16.4	16.9	1.3	1.4	1.5	+7.0	-13.9	16.8
006	15.6	20.2	16.1	23.6	22.4	20.4	10.5	14.3	17.7	1.3	1.4	1.5	+5.8	-13.9	16.5
009	16.0	18.0	15.4	23.6	22.3	20.3	10.6	14.1	15.8	1.3	1.4	1.5	+2.5	-15.0	16.4
012	13.5	16.5	16.1	23.4	22.1	20.1	12.4	17.5	17.7	1.3	1.4	1.5	+4.0	-14.1	16.1
016	15.1	20.4	18.3	23.3	22.2	20.2	10.0	13.0	16.8	1.3	1.4	1.5	+3.9	-14.3	16.2
017	15.5	21.2	17.7	23.5	22.4	20.5	9.6	13.4	17.7	1.4	1.4	1.5	+6.9	-14.0	16.7
019	14.2	19.3	18.0	23.6	22.4	20.5	11.2	15.4	18.6	1.3	1.4	1.5	+3.6	-14.5	15.8
023	14.5	20.0	19.5	23.6	22.4	20.4	11.3	15.5	16.9	1.3	1.4	1.5	+6.1	-14.1	16.2
029	15.6	17.2	14.7	23.5	22.2	20.2	10.9	14.4	16.5	1.3	1.4	1.5	+4.5	-14.3	16.3
036	16.1	19.0	15.7	23.1	21.8	19.9	11.2	15.2	17.1	1.3	1.4	1.5	+4.6	-14.0	15.8
041	15.6	17.7	14.8	23.3	21.9	20.0	11.5	14.7	15.9	1.3	1.4	1.5	+4.2	-14.1	16.1
	⇓	⇓	⇓	⇓	⇓	⇓	⇓	⇓	⇓	⇓	⇓	⇓	⇓	⇓	⇓
Min	**13.5**	**16.5**	**14.7**	**23.1**	**21.8**	**19.9**	**9.6**	**13.0**	**16.3**	**1.3**	**1.4**	**1.5**	**+2.5**	**-15.0**	**15.8**
Max	**16.9**	**21.2**	**19.5**	**24.0**	**22.7**	**20.6**	**12.4**	**17.5**	**17.7**	**1.4**	**1.4**	**1.5**	**+7.0**	**-13.9**	**16.8**
Mean	**15.3**	**19.0**	**16.4**	**23.5**	**22.2**	**20.3**	**10.9**	**14.7**	**17.0**	**1.3**	**1.4**	**1.5**	**+5.0**	**-14.2**	**16.3**
Std. Dev. σ_n	**0.87**	**1.57**	**1.49**	**0.21**	**0.24**	**0.20**	**0.77**	**1.30**	**0.79**	**0.03**	**0**	**0**	**1.4**	**0.30**	**0.30**

Note: Population Standard Deviation is used (σ_n), not sample standard deviation (σ_{n-1})

Appendix B. Data Plots for the two-stage BFP640 5 – 6 GHz LNA. (From one sample PC Board).

Noise Figure Plot for complete two-stage cascaded LNA. T = 25°C.

Rohde & Schwarz FSEK3

13 Mar 2003

Noise Figure

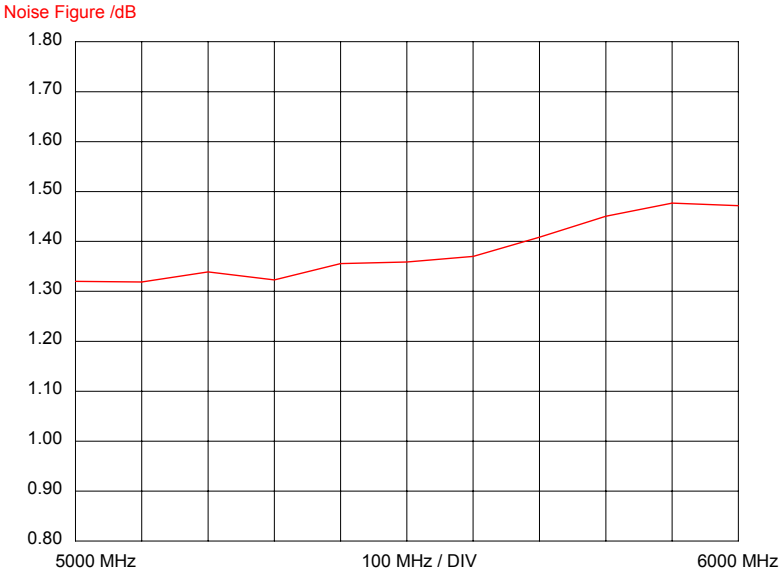
EUT Name:	Two Stage BFP640 5 - 6 GHz Low Noise Amplifier
Manufacturer:	Infineon Technologies
Operating Conditions:	V = 3.3 V, I = 16 mA, T = 25 C
Operator Name:	Gerard Wevers
Test Specification:	AN082
Comment:	On BFP640 PCB 640-052402 Rev C 10 March 2003

Analyzer

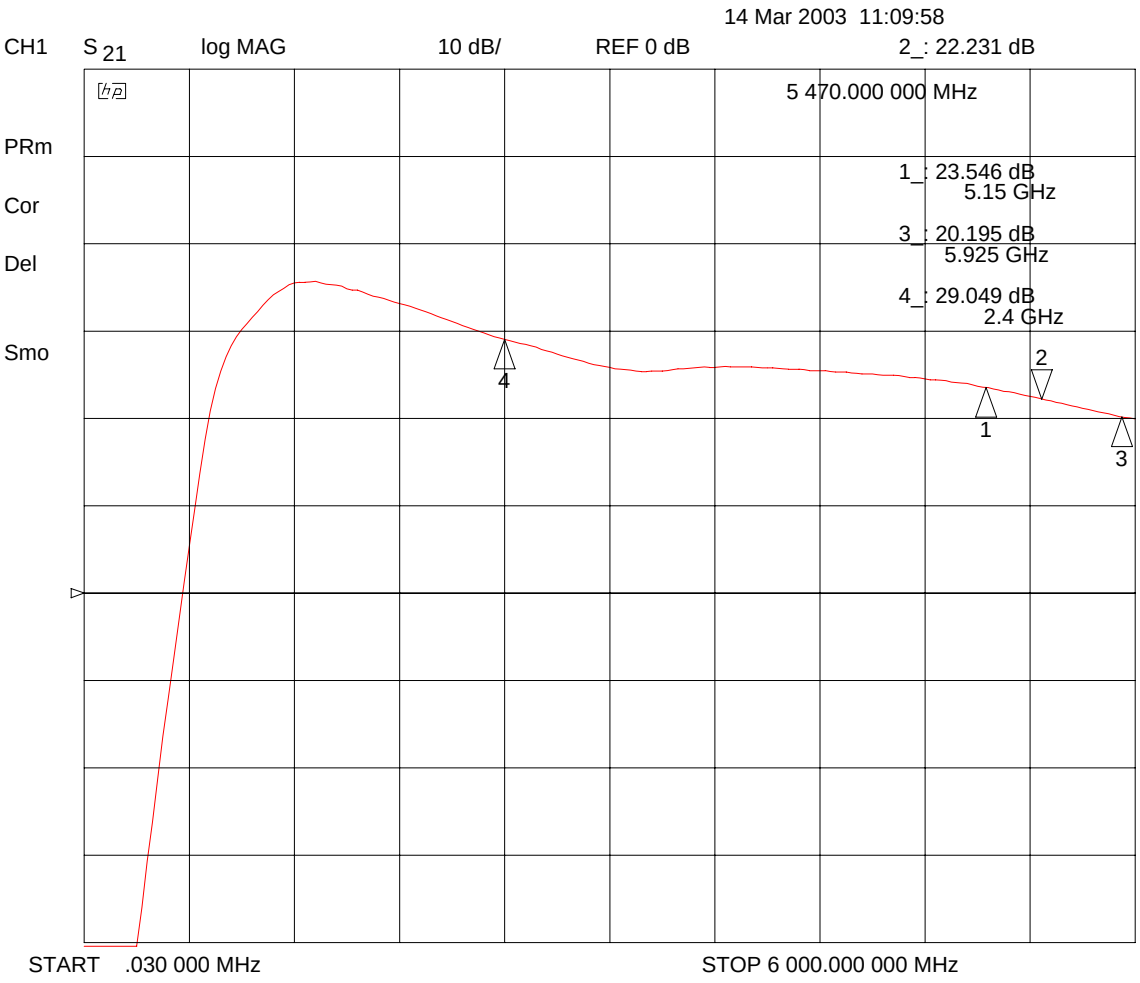
RF Att: 0.00 dB	RBW : 1 MHz	Range: 30.00 dB
Ref Lvl: -54.00 dBm	VBW : 100 Hz	Ref Lvl auto: ON

Measurement

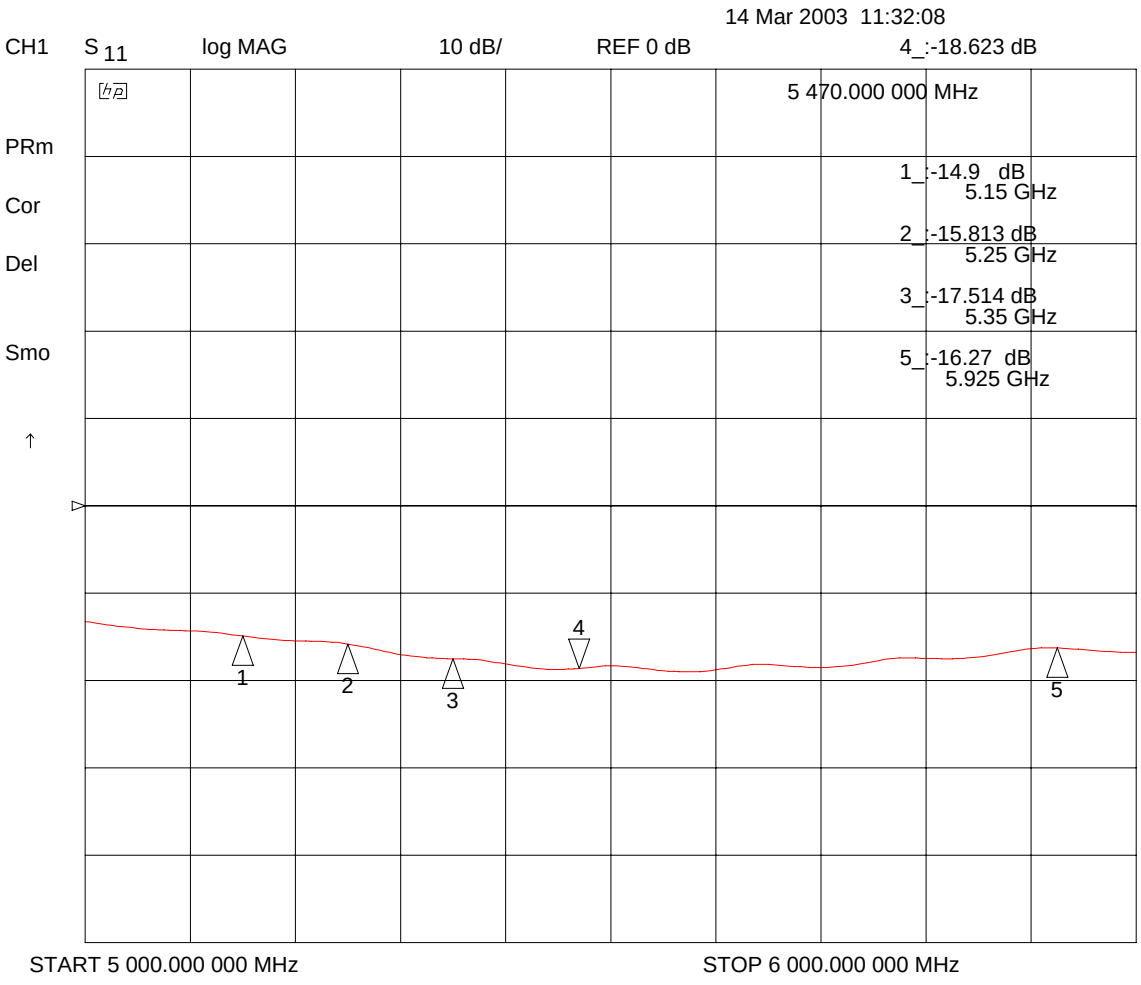
2nd stage corr: ON	Mode: Direct	ENR: HP346A.ENR



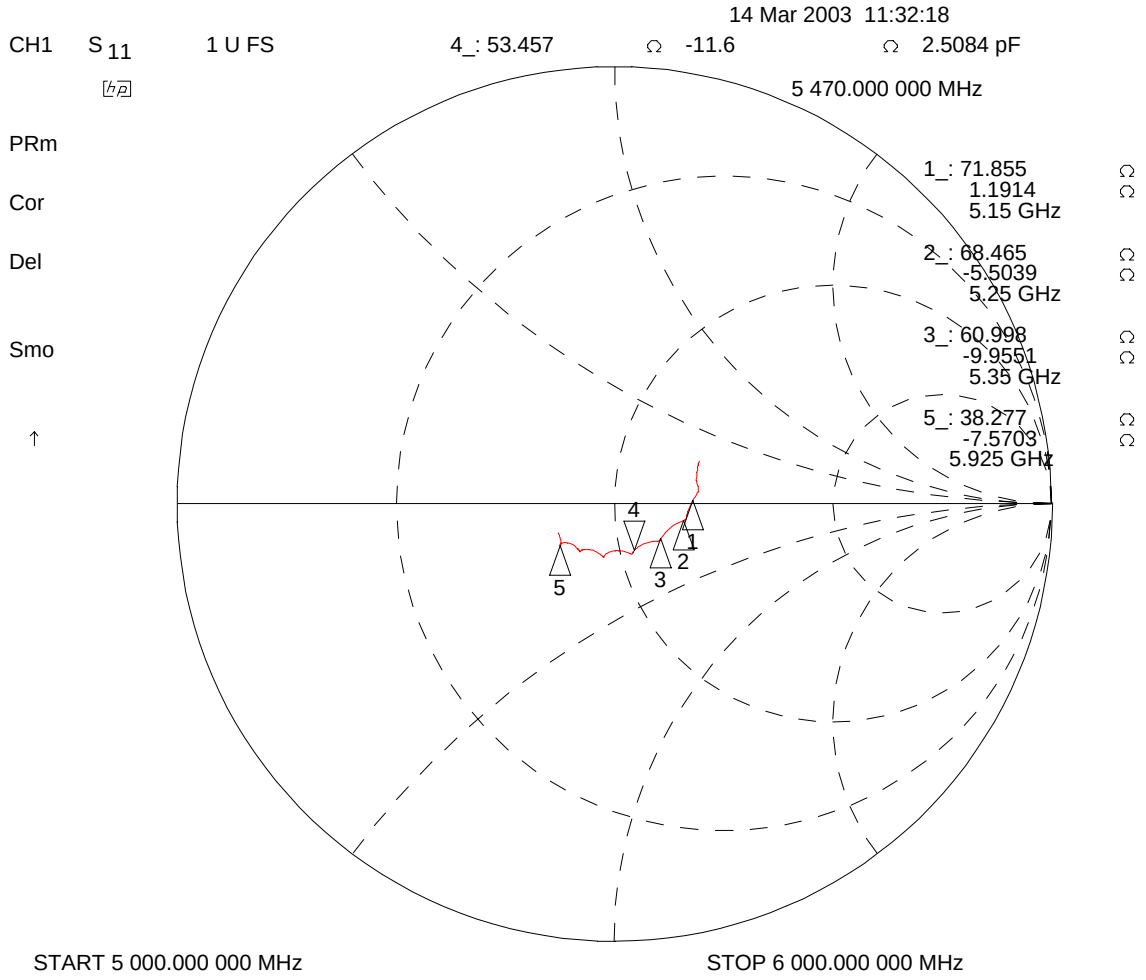
Forward Gain, Wide Span
(30 kHz – 6 GHz)
T = 25°C.



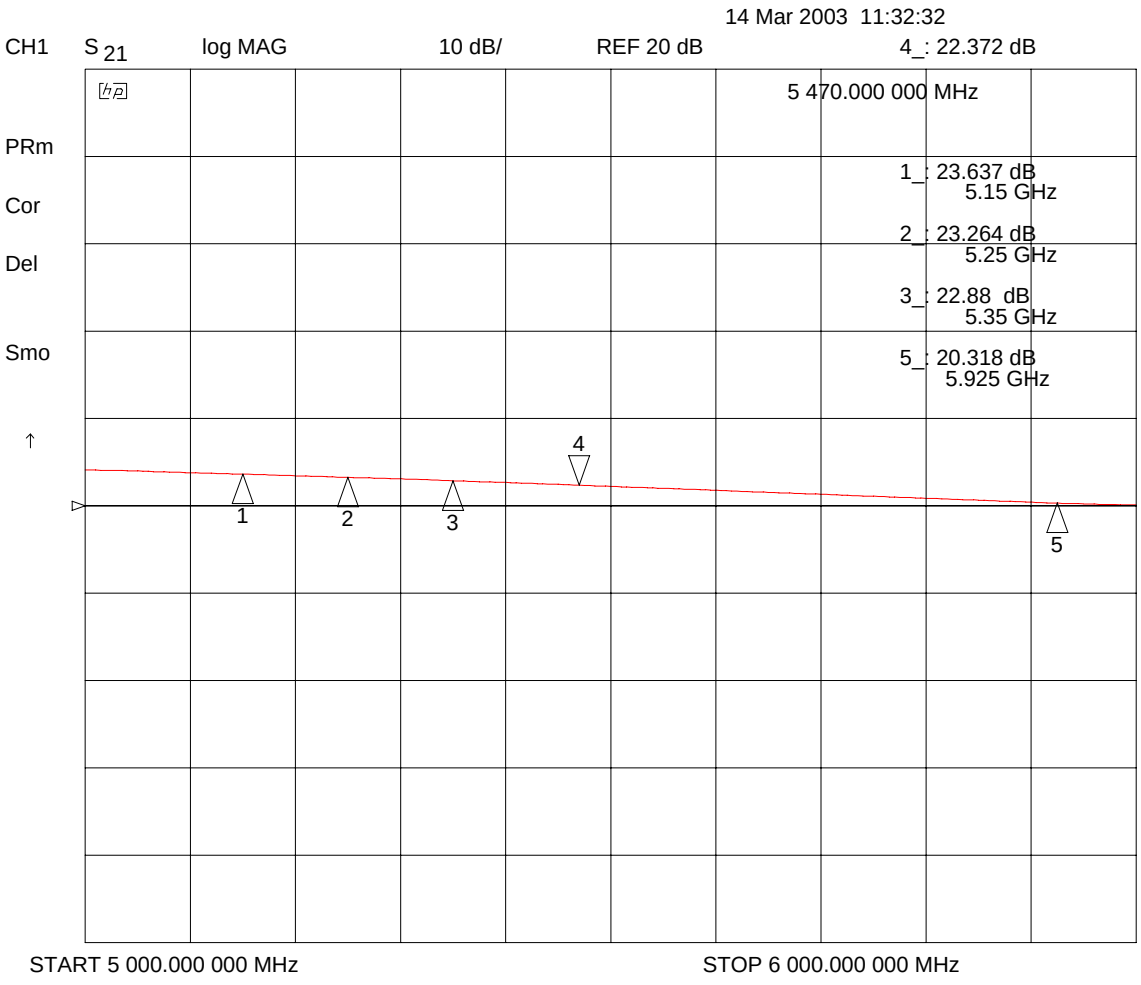
Input Return Loss, Log Mag, Narrow Span.
(5 – 6 GHz).
T = 25°C.



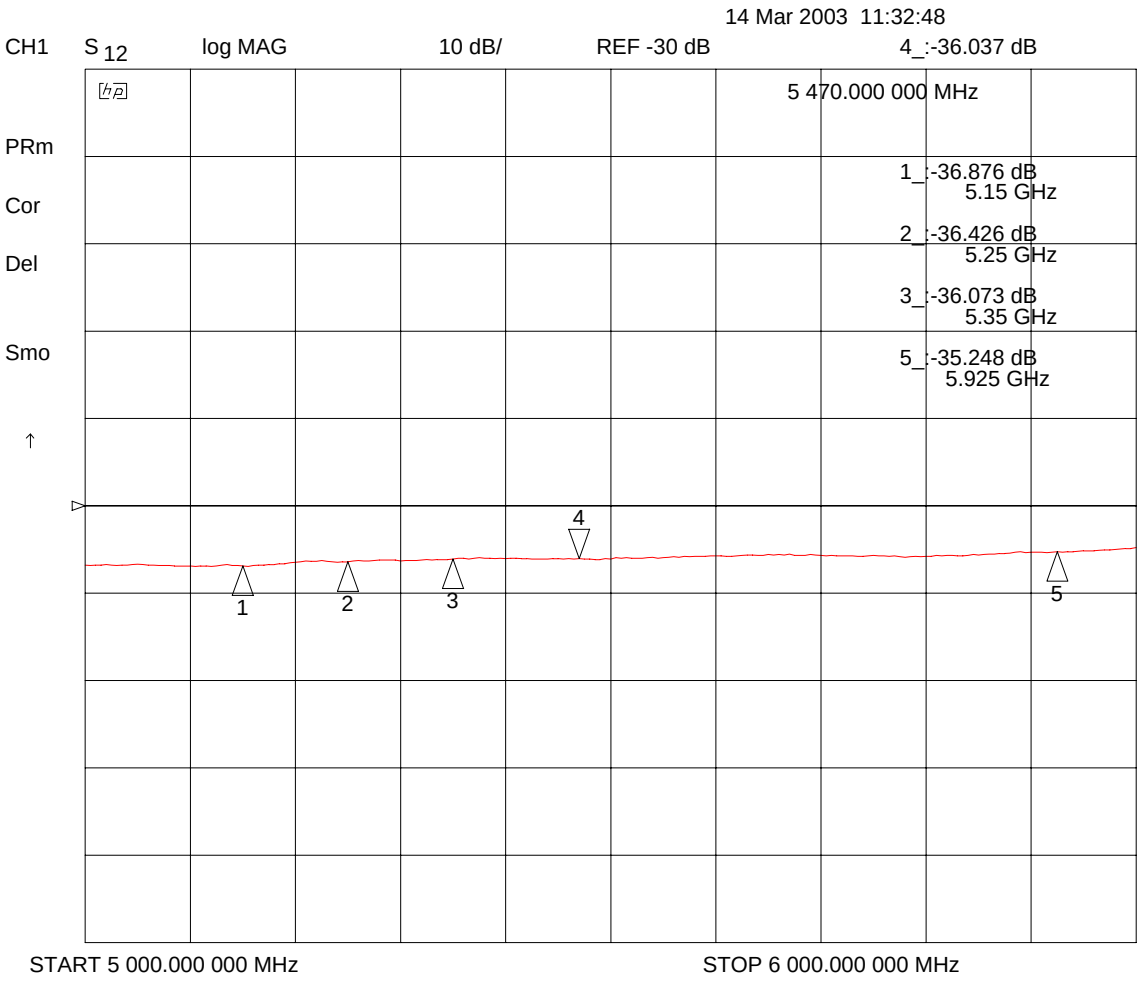
Input Return Loss, Narrow Span, Smith Chart.
(5 –6 GHz, Reference Plane = PCB Input SMA Connector)
T = 25°C.



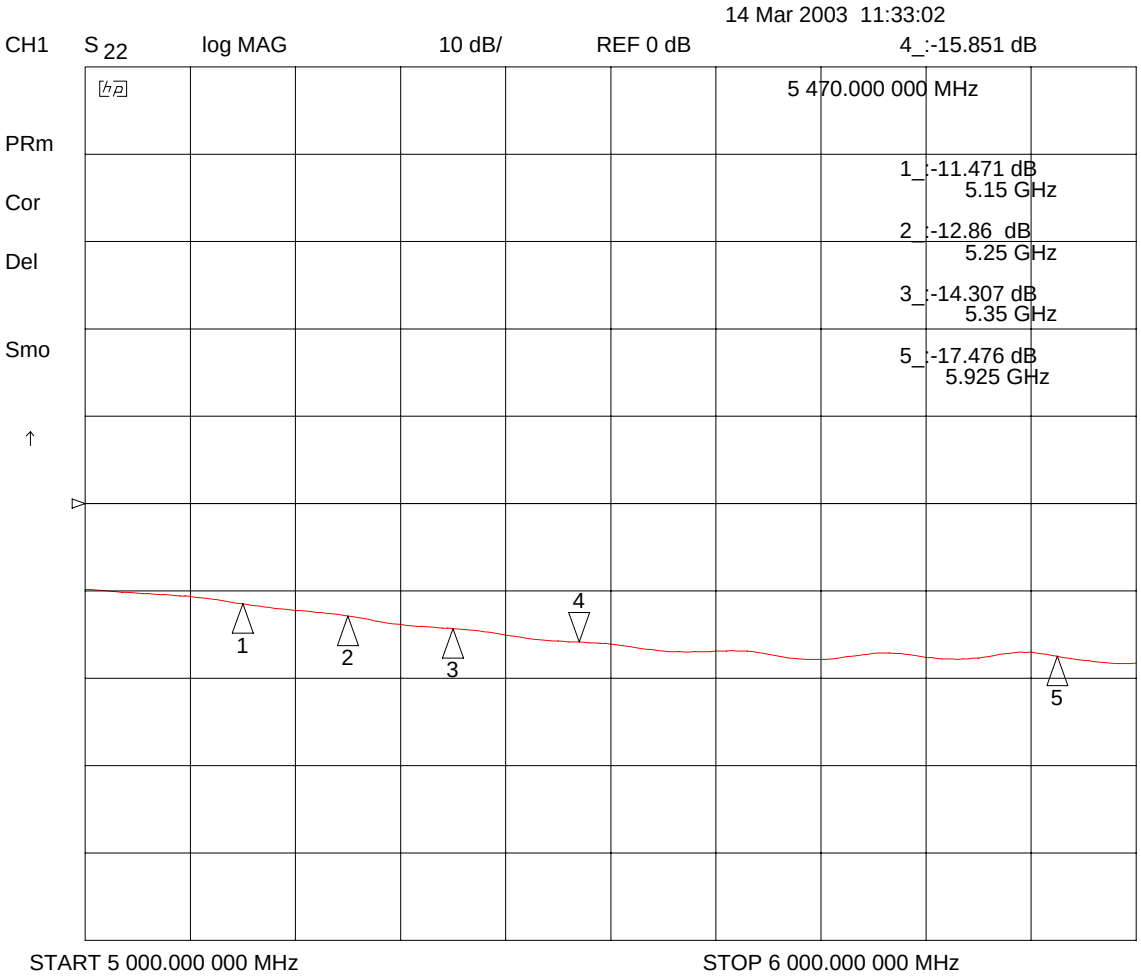
Forward Gain, Narrow Span.
(5 – 6 GHz)
T = 25°C.



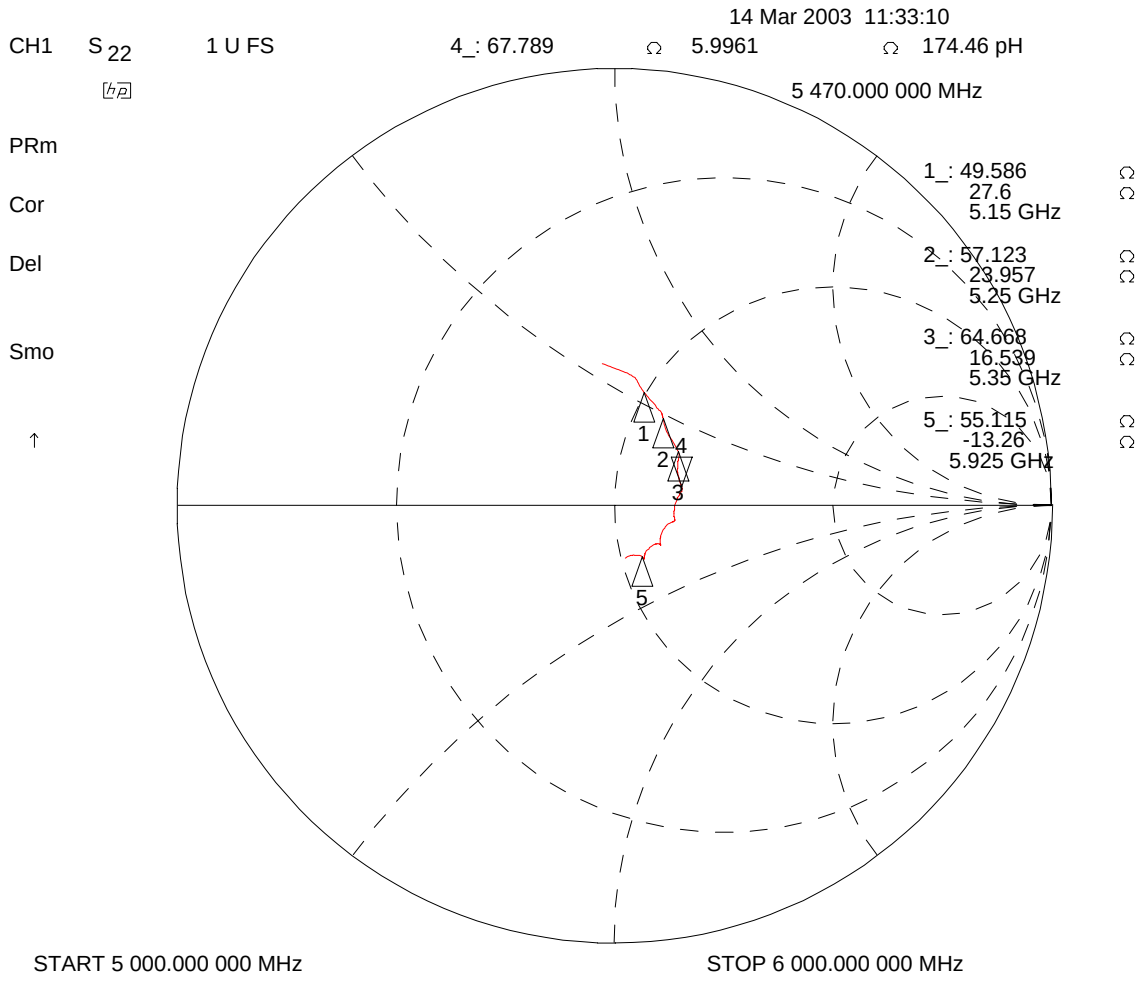
Reverse Isolation, Narrow Span.
(5 – 6 GHz)
T = 25°C.



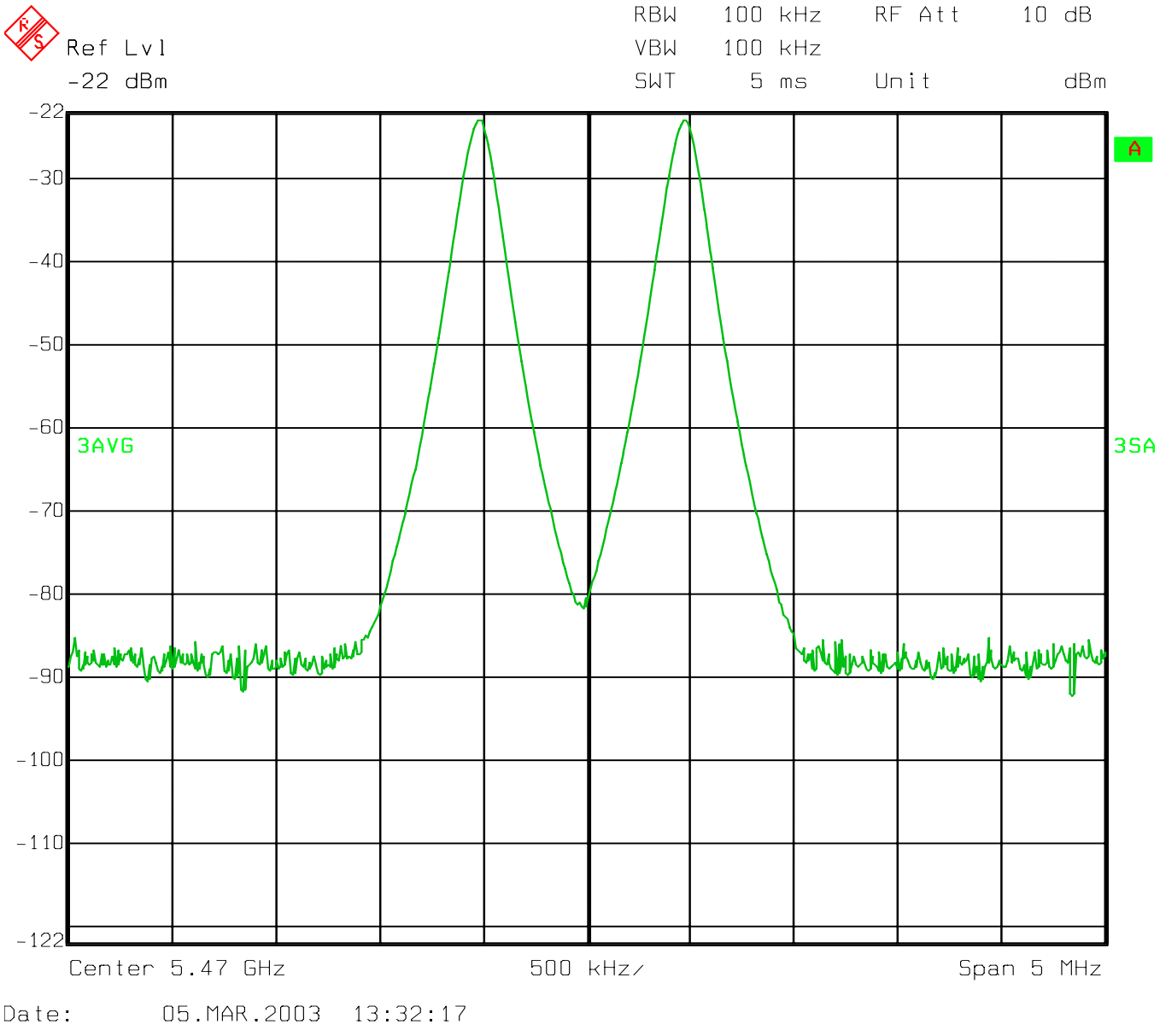
Output Return Loss, Log Mag, Narrow Span
(5 – 6 GHz)
T = 25°C.



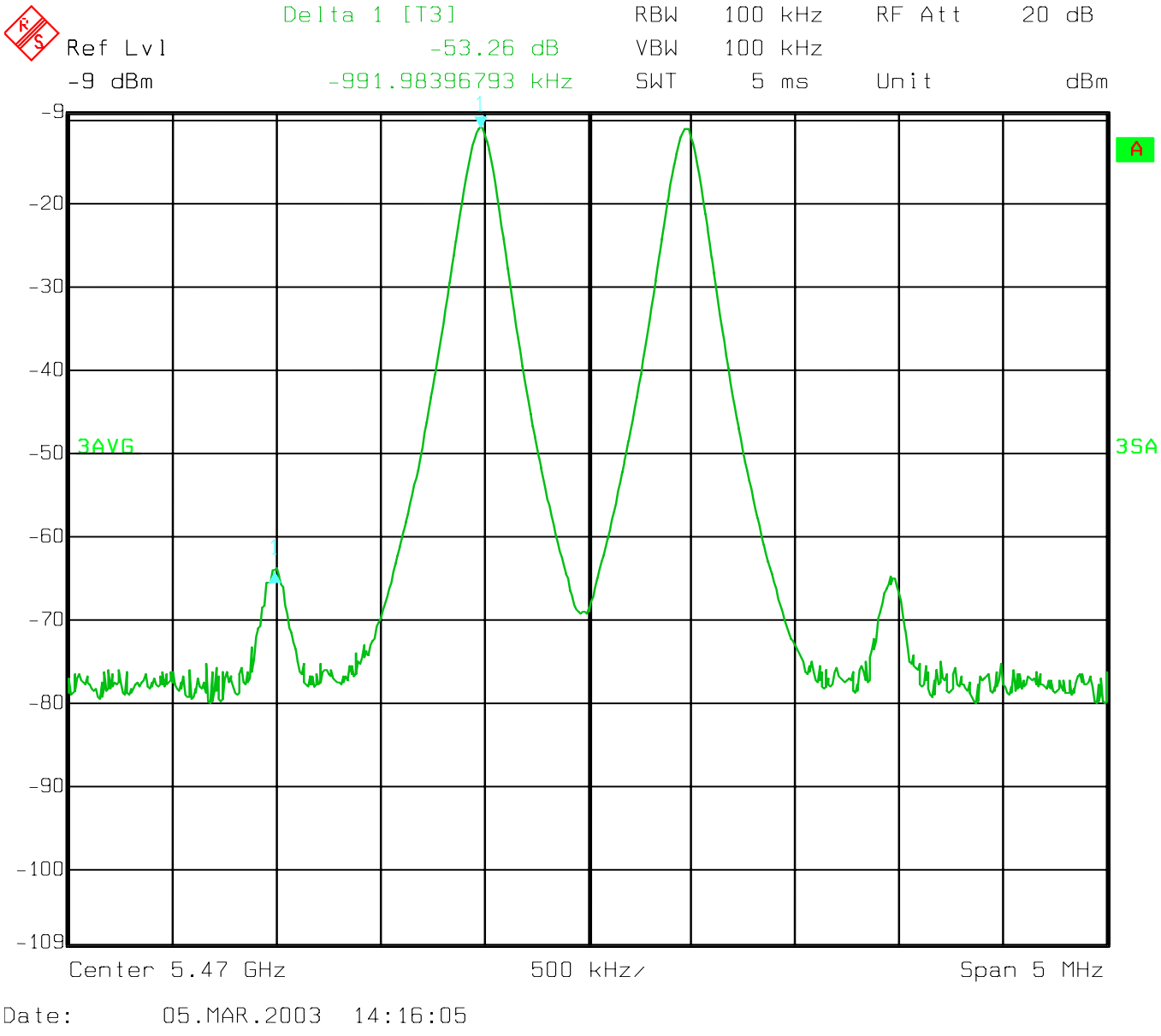
Output Return Loss, Narrow Span, Smith Chart.
(5 – 6 GHz, Reference Plane = PCB SMA Output Connector)
T = 25°C.



Input Stimulus for Two-Tone Third Order Intercept Test. Two Tones, 5469.5 MHz and 5470.5 MHz, - 23 dBm power per tone. T = 25°C.



Two-Stage LNA Output Response to Two-Tone Test.
Input 3rd Order Intercept = -23 + (53.3 / 2) = +3.7 dBm.
T = 25°C.



Appendix C. Temperature Test Data for one sample unit.

Single LNA Stage ONLY (Stage 1):

Temperature °C	Frequency MHz	dB $[S11]^2$	dB $[s21]^2$	dB $[s12]^2$	dB $[s22]^2$	I_{DC} mA
	5150	17.1	11.8	17.8	11.4	---
-40	5470	18.1	11.4	17.3	14.4	8.4
	5925	17.9	10.8	16.6	16.9	---
	5150	15.4	11.3	18.2	10.4	---
+25	5470	18.5	10.9	17.7	13.2	7.7
	5925	18.7	10.3	17.0	15.2	---
	5150	13.5	10.7	18.5	9.5	---
+85	5470	17.8	10.4	18.0	12.2	7.2
	5925	20.7	9.8	17.4	14.3	---

Conclusions:

1) Gain change vs. temperature is approximately -0.008 dB / °C (≈1 dB gain change cold to hot)
2) Current change over full temperature range is 1.2 mA, or 16%
3) Slight degradation in output return loss when hot

Two-Stage LNA (another unit; both stages in cascade):

Temperature °C	Frequency MHz	dB $[S11]^2$	dB $[s21]^2$	dB $[s12]^2$	dB $[s22]^2$	I_{DC} mA
	5150	15.6	23.9	35.5	11.2	---
-40	5470	15.6	22.6	35.0	15.8	16.2
	5925	14.3	20.9	33.3	21.7	---
	5150	17.1	23.1	35.7	10.2	---
+25	5470	17.9	21.8	35.8	14.9	15.0
	5925	14.5	19.9	35.2	23.0	---
	5150	17.8	22.2	37.2	9.6	---
+85	5470	22.1	20.8	36.7	14.7	14.2
	5925	15.2	18.8	36.5	25.0	---

Conclusions:

1) Gain change vs. temperature is approximately -0.014 dB / °C (1.8 dB change cold to hot)

2) Current change over full temperature range is 2.0 mA, or 13%

Appendix D. Revision Log

Revision Level	Date	Description of Modification(s)
A	14 March 2003	Initial Release
B	17 March 2003	Cleanup
C	19 March 2003	Addition of temperature test data (Appendix C).
D	26 March 2003	Cleanup of Figure 2, page 3.